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HANLEY, FLIGHT & ZIMMERMAN, LLC
20 N. WACKER DRIVE
SUITE 4220
CHICAGO, IL 60606

EXAMINER	
PEUGH, BRIAN R	
ART UNIT	**PAPER NUMBER**
2187	

DATE MAILED: 06/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/073,492	EDIRISOORIYA ET AL.	
	Examiner	Art Unit	
	Brian R. Peugh	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 March 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *8,9,14-16,26 and 27* is/are allowed.

6)☒ Claim(s) *1-7,10-13,17-25 and 28-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 February 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/24/05,8/26/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

This Office Action is in response to applicant's communication filed March 24, 2005, and August 26, 2004, in response to PTO Office Action dated May 21, 2004. The applicant's remarks and amendment to the specification and/or claims were considered with the results that follow. The March 24, 2005 response is a duplicate of the August 26, 2004 response.

Claims 1-32 have been presented for examination in this application. In response to the last Office Action, claims 1, 4, 7-10, 13, 17-19, 22-24, 26-28, 31, and 32 have been amended.

The Examiner acknowledges Applicant's change of status of the current application to that of a continuation-in-part of a previous application. The Applicant has complied with the requirements of 35 U.S.C. 120 for claiming benefit of an earlier nonprovisional application for the current application as a continuation-in-part, as found in MPEP 201.08.

Information Disclosure Statement

The information disclosure statements (IDS) submitted on May 24, 2005 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner. The IDS of August 26, 2004, will not be considered as it contains the same references as that of the May 24, 2005 IDS.

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "arbitration circuit enforcing a fixed cache intervention priority" (Claim 10) must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: The claims recite the limitations of "a predetermined arbitration hierarchy" (independent claims 1, 17, and 28), "an arbitration circuit enforcing a fixed cache intervention priority" (Independent claim 10), and "a predetermined hierarchy" (Independent claim 24).

Claim Objections

Claims 1-7, 17-25, and 28-32 are objected to because of the following informalities:

Claims 1, 17, and 28 recite "a predetermined arbitration hierarchy", while claim 24 recites "a predetermined hierarchy". The Specification fails to recite or disclose an arbitration system according to the aforementioned claim terminology. After consulting Applicant's Specification as well as Applicant's response of March 24, 2005, however, the Examiner believes that the predetermined (arbitration) hierarchy as claimed refers to the hardware system as described in paragraph 0021 of Applicant's Specification. The Examiner has interpreted the agent with the B_OFF input with logic zero as having the highest (predetermined) priority, with the other agents having a cascading (predetermined) priority due to the logical OR gates as seen in Figure 2 and recited in paragraph 0021. The Examiner will interpret claims 1-7, 17-25, and 28-32 according to this interpretation.

The Applicant is encouraged to amend the claims in such a fashion that the claim limitation terminology has clear antecedent basis within the Specification.

Claims 2-7, 18-23, 25, and 29-32 are objected to as being dependent upon a previously objected claim.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 10-13 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claim 10 recites "...an arbitration circuit enforcing a fixed cache intervention priority between the first processing agent, the second processing agent and the third processing agent". The Specification fails to recite an 'circuit' responsible for arbitration and enforcing a 'fixed cache intervention priority' system between the three processing agents.

Claims 11-13 are rejected as being dependent upon a previously rejected claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-7, 17-19, 24, 25, and 28-32 are rejected under 35 U.S.C. 102(e) as being anticipated by Chang (US# 6,519,685).

Regarding claim 1, Chang teaches **cache intervention** (the updating of modified data) by **reading a memory block** (line) **from main memory into the cache** of caching agent #1, **copying the memory block from the first cache to a second cache in response to a read request associated with the second cache** [Agent #1 is responsible for providing (copying) the memory block (line) to Agent #2 (col. 9, lines 49-53 & 66 – col. 10, line 4) due to the non-modified (Exclusive) state of the data.] and **tagging** (marking) **the line in the first cache as non-modified** (Exclusive) (col. 8, line 65 – col. 9, line 4; col. 4, lines 46-53). Chang further teaches **detecting a read request for the cache block (line) by a third cache (agent) that hits the first cache and the second cache** [Both cache (agents) **#1 and #2 hold the data in a non-modified state**], and the system of Chang **determines (arbitrates) that caching agent #1 will supply the data to caching agent #3 due to the tagged state of the data in caching**

agent #1. The **memory block (line) is copied to cache (agent) #3 from cache #1, which was the predetermined arbitration winner** [arbitration winner due to state of data based on predetermined cache coherency rules; see also (col. 9, lines 49-53 & 66 – col. 10, line 4)].

Regarding claim 2, and as recited above, Chang teaches that the **loading of the cache block (line) into the cache from the main memory includes tagging the line as Exclusive** (col. 6, lines 36-39; col. 8, line 65 – col. 9).

Regarding claim 3, according to the claim limitations the "tagging" operation is not required to immediately follow the "reading" operation. As such, operations may have occurred before the claimed "tagging" operation, such as first tagging the loaded memory block (line) as "Exclusive", followed by the request from another agent (agent #2) for the "Exclusive" data. Chang teaches that the first agent will provide the memory block (line) to the another agent, at which point **the non-modified memory block (line) will be tagged as "Shared",** in accordance with the claim limitation. These steps are seen in column 9, lines 5-24, such that the operations following the "tagging" operation of the parent claim now correspond to caching agent #3.

Regarding claim 4, Chang teaches that the memory block (line) of **caching agents** #1 and **#2 are tagged as Shared** in response to the read request (col. 9, lines 9-14).

Regarding claim 5, Chang teaches **that detecting a read request includes snooping a bus** for the corresponding transaction data (col. 3, lines 29-35 & 58-67; col. 4, lines 32-36; col. 9, lines 5-14).

Regarding claim 6, Chang teaches that **a directory indicating the lines copied from main memory to a processors cache is used during the snoop read request by a second agent** (col. 10, lines 32-47 & line 66 – col. 11, line 17).

Regarding claim 7, Chang teaches the memory block (line) is copied to cache (agent) #3, which is required before the **memory block (line) of cache (agent) #3 can be tagged as non-modified** (Shared) (col. 9, lines 15-24; col. 7, lines 8-22).

Regarding claim 17, Chang teaches that each "caching agent" has caching capabilities, such as a processor. As seen in Figure 1, **a first microprocessor** [CPU 1] **includes a first cache** [cache 1] **and a second microprocessor** [CPU 2] **includes a second cache** [cache 2], **where the first cache stores a copy of a memory block** [cache line] **in a non-modified** [exclusive] **state** (col. 9, lines 1-2 & 7). The second cache (agent) **stores the second copy of the memory block in the non-modified** (shared) **state** [col. 9, lines 12-13]. Chang teaches detecting a read request for the cache block (line) **by a third cache (agent) and third microprocessor** [col. 9, lines 15-16]. **A**

main memory is coupled to the first microprocessor, second microprocessor, and third microprocessor [Fig. 1; shared main memory (106)]. **The first microprocessor or second microprocessor is responsible for providing the memory block (line) to the third cache of the third microprocessor based on a predetermined arbitration hierarchy while the first copy of the memory block** (shared-respond) **and the second copy** (shared) **of the memory block are in the non-modified state.** [The system of Chang determines (arbitrates) that caching agent #1 will supply the data to caching agent #3 due to the tagged state of the data in caching agent #1. The memory block (line) is copied to cache (agent) #3, which is required before the memory block (line) can be tagged as non-modified (Shared) (col. 9, lines 15-24; col. 9, line 66 – col. 10, line 4; col. 7, lines 8-22). The arbitration winner is due to state of data based on predetermined cache coherency rules; see also (col. 9, lines 49-53 & 66 – col. 10, line 4)].

Regarding claim 18, Chang teaches that **the first microprocessor will supply the second cache with the second copy of the memory block** (cache line) **while the first memory block** (cache line) **is in one of an exclusive state** or shared state (col. 10, lines 1-4).

Regarding claim 19, Chang teaches **wherein the main memory is operatively connected to the first microprocessor and second microprocessor** [shared main memory (106)] **by a main memory bus** [(108)].

The **first microprocessor will directly supply the second cache with the second copy of the memory block** (cache line) **while the first copy is in the non-modified** (exclusive) **state** without the use of the main memory (col. 9, lines 57-65).

Regarding claim 24, Chang teaches **storing a memory block** (cache line) **stored in a first cache** (of the snooping agent) **is in a shared**-respond **state** (col. 10, lines 25-31; col. 3, lines 29-36). The second cache (agent) **stores the second copy of the memory block in the non-modified** (shared) **state** [col. 9, lines 12-13]. The snooping agent **detects a read request associated with the memory block by an agent** [requesting agent] **associated with a second cache** [of the requesting agent] **while the memory block in the first cache** [of the snooping agent] **is in the shared**-respond **state**. The snooping agent is responsible for **copying the memory block from the first cache to the second cache in response to detecting the read request while the memory block in the first cache is in the shared state** (col. 10, lines 26-31).

Selecting the first cache or the second cache to provide a copy the memory block (line) to the third cache based on a predetermined arbitration hierarchy, and copying the memory block to the third cache in accordance with the selection. [The system of Chang determines (arbitrates) that caching agent #1 will supply the data to caching agent #3 due to the tagged state of the data in caching agent #1. The memory block (line) is copied to cache (agent) #3, which is required before the memory block (line) can be tagged as

non-modified (Shared) (col. 9, lines 15-24; col. 9, line 66 – col. 10, line 4; col. 7, lines 8-22). The arbitration winner is due to state of data based on predetermined cache coherency rules; see also (col. 9, lines 49-53 & 66 – col. 10, line 4)].

Regarding claim 25, Chang teaches that if another cache has the memory block (cache line) in a shared state, this cache will not be responsible for supplying the data to the requestor (col. 8, lines 26-31). The cache with the data in the shared-respond state is required to supply the data to the requestor if more than one cache contain the memory block (col. 10, lines 26-31; col. 7, lines 8-13). Therefore, **a third cache** (such as cache N of CPU N; Fig. 1) **with the memory block** (cache line) **is prevented from copying the memory block** (cache line) **to the second cache** (requesting agent) because the third cache has the memory block in a shared state and not a shared-respond state.

Regarding claim 28, the Examiner will interpret the claimed 'second cache' and 'second copy' as the 'third cache' and 'third copy', respectively. Also, the Examiner will interpret the claimed 'third cache' and 'third copy' as the 'second cache' and 'second copy', respectively. This is done to demonstrate the claimed similarities of claim 28 with independent claims 1, 17, and 24. The interpretation does not deviate from the claimed subject matter, but rather is done to illustrate that by switching the numbering of the caches and data block copies, the claimed

subject matter has already been taught by Chang as described previously in claims 1, 17, and 24.

Regarding claim 28, Chang teaches **storing a first copy of a memory block** (line) **into the first cache** of caching agent #1 **in one of an exclusive state or a shared state** [here, in the exclusive state (col. 8, line 65 – col. 9, line 4; col. 4, lines 46-53)]. Agent #1 **detects a memory read request corresponding to a second cache and associated with memory block** [interpreted as third agent and third claim(col. 9, lines 5-8).
The first agent is responsible for **supplying the second** (third) **cache with a second** (third) **copy of the memory block (line) while the first copy of the memory block is in one of the exclusive state and shared state without accessing main memory** (col. 9, line 57 – col. 10, line 4), **and preventing a third** (second) **cache having a third** (second) **copy of the memory block from supplying the second** (third) **copy of the memory block to the second** (third) **cache if the first and third** (second) **copies of the memory block are in the shared state and the first cache has a higher cache intervention priority under a predetermined hierarchy** [The system of Chang determines (arbitrates) that caching agent #1 will supply the data to caching agent #3 due to the tagged state of the data in caching agent #1. The memory block (line) is copied to cache (agent) #3, which is required before the memory block (line) can be tagged as non-modified (Shared) (col. 9, lines 15-24; col. 9, line 66 – col. 10, line 4; col. 7, lines 8-22). The arbitration winner is due to state of data based on

predetermined cache coherency rules; see also (col. 9, lines 49-53 & 66 – col. 10, line 4)].

Regarding claim 29, Chang teaches **that detecting a read request includes snooping a bus** for the corresponding transaction data (col. 3, lines 29-35 & 58-67; col. 4, lines 32-36; col. 9, lines 5-14).

Regarding claim 30, Chang teaches that **a directory indicating the lines copied from main memory to a processors cache is used to detect the snoop read request by a second agent** (col. 10, lines 32-47 & line 66 – col. 11, line 17).

Regarding claim 31, Chang teaches that the first microprocessor will **directly supply the second cache with the second copy of the memory block** (cache line) **while the first copy is in the Exclusive** (non-modified) **state** (col. 9, lines 57-65).

Regarding claim 32, the snooping agent detects a read request associated with the memory block by an agent [requesting agent] associated with a second cache [of the requesting agent] while the memory block in the first cache [of the snooping agent] is in the shared-respond state. The snooping agent is responsible for **supplying the second cache with the second copy of the**

memory block while the memory block in the first cache is in the shared state (col. 10, lines 26-31).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 20-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang (US# 6,519,685) as applied to claims 1-7, 17-19, 24, 25, and 28-32 above, and further in view of O'Leary et al. (US# 5,867,162).

Regarding claim 20, the difference between the claimed subject matter and that of Chang, disclosed supra, is that claim 20 recites that a motherboard, hard drive and graphics (display) card are each coupled to the first microprocessor. As seen in Figure 2, O'Leary et al. teaches that the **motherboard** (204) **is coupled to the CPU**, and that the hard drive (212) and graphics (display) card (210) are coupled to the motherboard, and thus **the hard drive and graphics card are coupled to the CPU** (col. 3, lines 1-3). Therefore it would have been obvious to one of ordinary skill in the art having the teachings of Chang and O'Leary et al. before him at the time the invention was made to modify the cache coherency system of Chang to include the microprocessor (CPU) coupled system components of a motherboard, disk drive and graphics

card of O'Leary et al. because by coupling the motherboard, hard drive, and graphics card system components to the CPU, the CPU is able provide them with the necessary instructions and operations in order for the system components to operate.

Regarding claim 21, Chang teaches that **an output device** (CRT display) outputs data via the I/O unit, where the I/O unit **is coupled** (interconnected) **to a** first **processing unit** (col. 1, lines 16-21), and thus the output device is coupled to the first processing unit. Chang teaches that **an input device** (keyboard) inputs instructions via the I/O unit, where the I/O unit **is coupled** (interconnected) **to a** first **processing unit** (col. 1, lines 10-15), and thus the input device is coupled to the first processing unit.

Regarding claim 22, Chang teaches that **the input device comprises** at least one of **a keyboard**, a mouse, a track pad, an isopoint, a microphone, or a graphics tablet (col. 1, line 13).

Regarding claim 23, Chang teaches that **the output device comprises** at least one of **a display**, a printer, a modem, a network card, or a speaker (col. 1, lines 20-21).

Allowable Subject Matter

Claims 8, 9, 14-16, 26, and 27 are allowed over the prior art of record.

Response to Arguments

Applicant's arguments with respect to claims 1-7, 10-13, 17-25, and 28-32 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian R. Peugh whose telephone number is (571) 272-4199. The examiner can normally be reached on Monday-Thursday

from 7:00am to 4:30pm. The examiner can also be reached on alternate Friday's from 7:00am to 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks, can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 571-272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Brian R. Peugh
Patent Examiner
Art Unit 2187